Abstract

This paper describes a procedure to extract major SPICE parameters of a field-effect transistor (JFET, MESFET or MOSFET) from its transfer and output i-v characteristics while introducing a technique that facilitates an accurate measurement of these characteristics with the help of standard bench-top electronic test equipment in a computer-integrated-electronics laboratory. The measurement technique, by requiring the availability of a function generator and only one digital-multi-meter (DMM) creates a means to do a quick and inexpensive determination of the SPICE parameters of field-effect transistors in-situ for computer-assisted electronics design. The technique and the extraction procedure have been tested and incorporated into the electronics laboratory experiments at the University of Southern Maine.

1. Introduction

One of the major challenges of undergraduate engineering instruction is to provide the student with a realistic and contemporary design experience while avoiding expensive special purpose test and measurement equipment. Following an earlier trend in the electronics industry, recent introduction into the electrical engineering curriculum of electronic design automation and simulation tools such as SPICE has created a need for an in-house capability for fast and accurate measurement of semiconductor device SPICE parameters.

SPICE is the most widely used electronic circuit simulation tool. Its wide acceptance as an industry standard for analog circuit simulation and electronic design verification is mostly due to its sophisticated device models which are based on device physics and yield accurate representation of device terminal behavior [1,2,6]. These models which include parasitic resistances and capacitances and important second order phenomena such as the "channel-length modulation" command for an accurate measurement of the terminal i-v characteristics of a device in order to be able to extract a realistic set of its numerous model parameters. However, specialized test equipment for measuring device characteristics such as Hewlett-Packard's HP4145A transistor parameter analyzer are prohibitively expensive. For instructional purposes such specialized equipment may also deprive the student of an opportunity to gain insight into the measurement process and understanding of the principles of device modeling. Use of standard electronic test-bench equipment which includes a digital-multi-meter (DMM), a function generator and a digital-storage oscilloscope is most desirable as long as a high level accuracy is obtained and the measurements are automated for sufficient data to be gathered in a reasonable time. In a modern computer-integrated electronics laboratory these conditions are easily met except for the simultaneous measurement of current/voltage or voltage/voltage pairs required for i-v characterization [10].

Guvench [5] described techniques of measuring the terminal i-v characteristics of two- or multiple-terminal bipolar devices in floating-terminal and common-terminal configurations. In these techniques, an IEEE-488 interfaced DMM with its separate voltmeter and ammeter inputs connected to the device is remotely switched by a computer program between its ammeter and voltmeter modes to collect i-v data pairs each time the voltage is increased by a stepped function generator. During these measurement cycles the voltmeter and the ammeter connections are kept stationary on the circuit. In this manner, integrity of the measurement circuit and consistency of circuit resistances are maintained. This also permits the effects of finite meter resistances to be accounted for through software. Guvench also describes the procedures for extracting the SPICE parameters of bipolar junction transistors and diodes from the acquired data.

In the SPICE modeling of bipolar devices the model parameters can be extracted from two separately measured terminal i-v characteristics, input and output. However, SPICE models of the field-effect transistors like JFETs, MESFETs and MOSFETs require transconductive transfer characteristics in addition to the i-v characteristics measured at their output terminals.

In this paper, Guvench's techniques are extended to include the measurement of the transconductive transfer characteristics of FETs in order to facilitate in-situ parameter determination of
their SPICE models for computer-assisted electronic design. Circuit configurations and measurement techniques are described and a procedure for extracting FET SPICE parameters is described by using the experimental data obtained from a JFET with these techniques. Both the technique and the procedure have been adopted to serve in a preliminary experiment leading to analog circuit designs involving field-effect transistors in the junior electronics courses at the University of Southern Maine. The measurements reported here were done at USM's Computer-Integrated-Electronics Laboratory which is equipped with setups comprising of a Tektronix AFG5101 function generator, a Tektronix DM5120 digital multimeter, a Tektronix PS250 power supply, and a Hewlett-Packard HP54501 digital oscilloscope all GPIB interfaced to an ACMA 33MHz 386 PC [10].

2. Measurement of I-V Characteristics

2.1 Transfer Characteristics

The transfer characteristics of an FET are defined to be the drain current (ID) of the device measured under a number of constant drain-source bias conditions and plotted as a function of the gate-source voltage (VGS).

Figure 1 illustrates the circuit connection used to acquire and plot the transfer characteristics of a field-effect transistor with one DMM. Although the device under test (D.U.T.) shown in the figure is an N-channel JFET the same circuit can serve for all varieties (JFET, MESFET and MOSFET, depletion or enhancement) and both types (N-channel and P-channel) of field-effect transistors as long as the polarities and the range of the voltages applied and the direction of the protection diode connected are chosen properly.

In this circuit the transistor's drain-source bias is provided by a variable-voltage DC power supply and is measured with the digital multi-meter at the beginning of the data acquisition manually before the meter is dedicated to acquiring the gate voltage data in remote during the course of data acquisition. The gate voltage is supplied by the function generator ("AFG5101" or "Vstep" in the figure) which operates in the DC mode. "RGprotect" and "Dprotect" resistor-Zener-diode pair constitutes a voltage clipper to protect the gate from an accidental application of excessive voltage. JFETs need this protection against an accidental forward biasing of their gate junction. For MOSFETs the clipper is a protection against an electrostatic discharge damage to the gate. If the range of VGS has to cover both polarities, two silicon Zeners (VZ1 and VZ2) connected in series in opposite directions will extend the range from \[ -VZ1 \leq VGS \leq 0.7 \] with a single diode to \[ -(VZ1 + 0.7) \leq VGS \leq +(VZ2 + 0.7) \] with two.

The digital multimeter with its "Voltage" input connected to the gate measures "VG" the gate voltage when it is in the "DC VOLTS" mode. Its "Current" input ("I" in the figure) is connected to the source of the device, therefore, it provides a short path to the drain current "ID" to flow to ground through its small internal resistance, RMETER,I. When the meter is switched to its "DC AMPS" mode this drain current is measured. A program named CIE-IV.EXE written in compiled BASIC controls and steps the generator through a user specified gate voltage range and in each step collects i-v data from the meter via GPIB. The program interprets the measured values as

\[
V_{GS} = V_{MEASURED} - (R_{METER,I} \cdot I_{MEASURED}) \quad (1)
\]

\[
ID = I_{MEASURED} \quad (2)
\]

where the second term in equation (1) is the voltage burden of
the ammeter due to its finite internal resistance. Although this drop can be kept small by using a higher range for the current it is best to eliminate its effect before it is misinterpreted in the SPICE parameter extraction process.

The data file generated by the "CIE-IV.EXE" is compatible in format with commonly used spreadsheet software like "QuatroPro" and can readily be converted into graphs. Figure 2 shows the transfer characteristics measured and graphed in this way. Typically the measurement of each i-v pair takes less than a second, with the actual time depending on the number of the digits of resolution (typically 6½) and the number of samples taken for averaging (typically 8) at each i-v point.

Figure 2 depicts two sets of ID vs VGS data, one taken at VDS=3V and the other at VDS=10V. Since the current reaches negligible values in -2.5V < VGS < 2.2V, the threshold of this device is estimated to be within that range. The drain bias voltages were intentionally chosen to be larger than the magnitude of this estimated threshold voltage so as to keep the operation in the saturation region. This choice makes extraction of some SPICE parameters easier, and also desensitizes the drain current to possible variations in VDS caused by the finite ammeter voltage drop in the VDS loop.

2.2 Drain Characteristics

The drain (or output) characteristics of a field-effect transistor is a set of ID vs VDS curves obtained under constant gate bias conditions. Figure 3 shows the circuit used in this work to measure ID and VDS by using only one meter. The gate bias is applied through a resistor-Zener-diode clipping circuit for protection against accidental application of excessive or forward biasing voltages to the gate. A variable DC supply (VGG) delivers bias voltage to the gate through this protection circuit.

The drain voltage is supplied by the computer controlled function generator which operates in the DC mode and its output is stepped over a user chosen range. R1, R2 are two resistors with precisely known resistances that help to measure the drain current. Note that the meter's "Voltage" input is connected to the drain, therefore, it measures VDS = V1 directly when it is operating in the "Voltmeter" mode. Its "current" input is connected to R2, therefore, it measures I2. The measured values of the current and the voltage are translated to device voltage and current by the data acquisition program according to the following equations.

\[
V2 = (R2 + R_{METER,I}) \cdot I_{2,MEASURED} \quad (3)
\]

\[
I1 = (V2 - V_{1,MEASURED}) / R1 \quad (4)
\]

\[
ID = I1 - (V_{1,MEASURED} / R_{METER,V}) \quad (5)
\]

\[
VDS = V_{1,MEASURED} \quad (6)
\]

ID and VDS values, when calculated tabulated and plotted, give the drain characteristics of the device.

Figure 4 is displaying the data acquired from an N-channel JFET (2N5951) at VGS = 0, -0.5V, -1.0V, -1.5V and -2.0V values.
3. SPICE Parameter Extraction

Although in detail they may differ, SPICE models of JFETs, MESFETs and MOSFETs all share a common square-law formula for the relationship between their terminal voltages and their drain currents \[1,2\]. This common relationship is rooted in the fact that, irrespective of the nature of the channel, whether the semiconductor inverted or depleted, the average charge accumulated in the channel due to the field-effect is proportional to the voltage applied to the gate. These relationships are mathematically described as,

\[ \text{ID} = \beta \cdot (2\cdot(V_{GS} - V_{TO}) \cdot V_{DS} - V_{DS}^2) \cdot (1 + \lambda V_{DS}) \quad (7) \]

\[ \text{ID} = \beta \cdot (V_{GS} - V_{TO})^2 \cdot (1 + \lambda V_{DS}) \quad (8) \]

Equation (7) applies in the linear region of the operation whereas equation (8) applies in the saturation region. These equations yield a continuous transition from one to the other at the onset of the drain current saturation. \((1 + \lambda V_{DS})\) factors tagged on to the square law part of the equations account for the finite slope of the drain characteristics in the saturation region. Since VDS and VGS dependencies are separated as multiplying factors in equation (8), it lends itself to parameter extraction more than equation (7). As a matter of fact equation (8), if interpreted as a function of VGS with VDS as a constant parameter rather than a variable, becomes exactly the device characteristics known as the transfer characteristics. For these reasons, if the transfer characteristics of the field-effect devices are obtained under drain saturation conditions the model extraction process becomes as simple as fitting equation (8) to the measured transfer characteristics.

However, with only a few VDS branches available the transfer characteristics cannot be used to check how closely ID vs VDS resembles the linear relationship implied by the model. The output characteristics of the device can serve better in finding the best \(\lambda\), i.e. the \(\lambda\) value that applies over a wide range of operation. In Figure 4 ID vs VDS curves are shown together with the dotted straight lines which stand for the linear \((1 + \lambda V_{DS})\) relation. These lines were generated and plotted by using the "Quattro Pro" spreadsheet program. In QuattroPro, from the ID and VDS columns a new column is created which calculates,

\[ \text{ID} = \text{ID}(@V_{DS}=5) \cdot \frac{(1 + \lambda V_{DS})}{(1 + \lambda 5)} \quad (9) \]

Note that equation (9) is nothing but equation (8) divided by itself calculated at \(V_{DS} = 5\) volts which is approximately the midpoint of the saturation region on the branches shown in Figure 4. Therefore, it is the equation of a straight line which intersects the branch at 5 volts. By varying \(\lambda\) these lines can be fitted to the saturation section of the characteristics. A \(\lambda\) value of 0.014 gave the best visual fit. Except near the tip of the \(V_{GS} = 0\) volt branch these straight lines are perfectly matching the curves. Noting that the tip mentioned corresponds to the highest power dissipation during the tests and the fact that mobility and ID decrease with junction temperature it is concluded that under constant junction temperature conditions the straight line drawn will actually be a better fit than it looks.

The transfer characteristics given by equation (8) implies the drain current to reach zero at \(V_{GS} = V_{TO}\). Therefore, \(V_{TO}\) can, in principle, be read off the transfer characteristics. However, this voltage by being at the bottom of a parabola cannot be identified accurately. \(V_{TO}\) would be much more precisely defined if it were defined to be the intersection of a straight line with the horizontal axis. Equation (8) can be converted into a straight line by taking a square-root of it. As a matter of fact, plotting \(\sqrt{\text{ID}}\) vs \(V_{GS}\) would also verify whether the device is behaving like predicted by the model. Figure 5 gives a plot of \(\sqrt{\text{ID}}\) plotted against \(V_{DS}\). Although this plot gives a much more precisely defined \((\text{ID} = 0)\) point for \(V_{TO}\), the curve deviates from the straight line prediction of the model, significantly.

![Figure 4. Measured FET Drain Chs.](image-url)
The deviation of the SQRT(ID) vs VGS from a straight line is due to the absence of a term that accounts for finite resistances of the bulk of the semiconductor at the drain and source terminations of the device structure. SPICE defines them to be RD and RS, respectively, and treats them as external resistances connected to a perfect device. In the transfer characteristics measured with drain in saturation, the effect of the voltage drop on RD will be negligible as long as (LAMBDA.RD.ID < < 1). But the voltage drop on RS, by being in the VGS loop, can distort ID vs VGS relationship. The distorted straight line behavior of the data points in Figure 5 clearly indicates a need to include RS in modeling this device. In the procedure outlined below for the extraction of VTO, BETA and RS the distortion seen in the transfer characteristics is assumed to be due to RS only and it yields excellent results.

1. Draw a tangent to the SQRT(ID) vs VGS curve at its maximum slope point which occurs at low currents when RS.ID drop is negligible. (see the dotted straight line in Figure 5)

2. The intersection of the tangent with VGS axis is VTO.

3. The slope of the tangent is SQRT( BETA.(1+ LAMBDA.VDS)). Use the LAMBDA value extracted earlier from the output characteristics and the VDS value under which the transfer characteristics was measured to calculate BETA.

4. Pick a point in the upper region of the curve. The horizontal distance between the tangent and the measured points is RD.ID. Calculate RD.

5. Verify the extracted values by creating a new column in the spreadsheet to calculate and plot

\[ f(VGS,ID) = \text{SQRT} \{ BETA.(VGS - RD,ID - VTO)^2.(1+ LAMBDA,VDS) \} \]

and compare the resulting curve (Model) with the data points.

6. Modify RS (and BETA and VTO) in small increments until the curve matches the data points over the whole range of ID.

The procedure outlined above yielded the curve labeled with "Model w/ RS" in Figure 5 and fits the data points very well. SPICE parameters obtained in this way are listed below.

\[
\begin{align*}
\text{BETA} & = & 2.015 \ \text{mA/V} \\
\text{VTO} & = & -2.40 \ \text{Volts} \\
\text{LAMBDA} & = & 0.014 \ \text{V} \\
\text{RS} & = & 82 \ \text{Ohms}
\end{align*}
\]

In Figure 2 two curves corresponding to the model with the above numbers and VDS = 3V and 10V are superimposed on the unconnected data point sets measured at the same drain voltage values. The agreement is obvious.

![Figure 5. SQRT(ID) vs VGS Plot](image)

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4. Pick a point in the upper region of the curve. The horizontal distance between the tangent and the measured points is RD.ID. Calculate RD.

5. Verify the extracted values by creating a new column in the spreadsheet to calculate and plot

\[ f(VGS,ID) = \text{SQRT} \{ BETA.(VGS - RD,ID - VTO)^2.(1+ LAMBDA,VDS) \} \]

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![Figure 6. Difference Between Measured and Model Currents](image)

**Figure 6. Difference Between Measured and Model Currents**

Figure 6 further testifies to the accuracy of the method as well as the square law SPICE model for the 2N5951 JFET measured. It displays the percentage deviation between the measured and the predicted drain currents. Note that the percentage error is below 1.1% for all points. It is observed that the largest deviations are found on the curve with higher VDS and when the device is passing the largest drain current, that is, the points where the device encountered higher power dissipation and increased junction temperature. Therefore, it is expected that the model will do even a better job for AC operations where the period of the signal is too short for the junction temperature to follow.

**4. Discussions and Conclusions**
A technique of measuring field-effect transistor transfer and output characteristics has been shown. The technique, adapted from a previously reported one for bipolar devices, eliminates the need for a second meter to be present for automated measurements. Thus, it creates an inexpensive means to measure and characterize field-effect transistors in an R&D or instructional laboratory to do in-situ characterization and SPICE model parameter determination for effective computer-assisted design.

A procedure for extracting SPICE parameters from such measurements has also been given by using data obtained from measurements on an N-channel JFET with excellent results. Although no other field-effect transistor examples are given, the technique and the extraction process are simple enough to adapt to any field-effect transistor, depletion or enhancement mode, JFET, MESFET or MOSFET, as long as gate leakages are small and the standard square-law SPICE models with parasitic resistances are applicable. It was observed that the source resistance distorts the square-law significantly. Therefore, it cannot be neglected. In analog amplifier designs, particularly those employing the FET in the common-source configuration SPICE simulations can be more than 30% in error in predicting the small-signal gain if a thorough determination of RS is not done in a process similar to the one presented here.

RD, the parasitic drain resistance is not, however, as important a parameter as RS in analog circuit design. This is because the voltage drop on RS creates a negative feedback effect in the VGS loop. The voltage drop on RD, being in the VDS loop, does not affect the drain current particularly if the device is operating in saturation. Its effect is simply to stretch the VDS axis in the output characteristics. Only in applications in which the field-effect transistor is driven near VDS = 0 (i.e. digital circuits) RD needs to be included in the model. In that case, the procedure presented above for RS can be repeated after reversing the source and the drain terminals to operate the transistor in an inverted configuration. For most devices, however, RD can safely be taken equal to RS with satisfactory results since most field-effect transistors have a drain-source symmetry.

The technique and the SPICE parameter extraction procedures presented in this paper have been tested and adopted in the junior electronics laboratory taught by the author at the University of Southern Maine where SPICE simulations are a requirement for experiments, most of which involve design-simulate-redesign-test-evaluate-redesign-... cycles.

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References


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The automated measurement system reported here employs a standard set of bench-top instruments consisting of a Hewlett Packard Digitizing Oscilloscope (Model 54501A), a Tektronix Arbitrary Function Generator (AFG 5101), and a Tektronix Programmable Digital Multimeter (DM 5120). All of these instruments are equipped with GPIB interface. [5] Guvench, M.G., “SPICE Parameter Extraction from Automated Measurement of JFET and MOSFET Characteristics in The Computer-Integrated-Electronics Laboratory”, Proc. of ASEE®'94, vol.1, pp.879-884. [6] Guvench, M.G., “Automated Measurement of MOS Capacitance and Determination of MOS Process Parameters in The MicroFabrication Laboratory® Proc. of ASEE, s2659, No.5, Milwaukee, 1997. SPICE, or Simulation Program with Integrated Circuit Emphasis, is a simulation tool for electronic circuits. You can convert some SPICE subcircuits into equivalent Simscape© Electrical© models using the Environment Parameters block and SPICE-compatible blocks from the Additional Components library. For more information, see subcircuit2ssc. Equation Variables. In the SPICE settings of the Environment Parameters block, specify the desired GMIN value for the GMIN parameter. Thermal Voltage, Vtn is the thermal voltage, which is defined as. Parameter extraction temperature, TMEAS © Parameter extraction temperature 300.15 K (default) | positive scalar. The temperature at which the transistor parameters are measured. The value must be greater than 0 K. The parameter extraction is usually performed by elaboration of experimental measurements, but some parameters are not directly measurable and others are not related to the physics of the device but are simply fit parameters to model the device as close as possible to reality. A Spice MOSFET model is the main switching element in the circuit. The other elements take into account the stray inductances due to the wires (Ls, Ld, Lg), the poly-silicon gate resistance (Rg), the resistance due both to silicon and to bonding (Rs, Rd), the body-drain capacitance modulation (DBD) and the leakage current when the device is in breakdown. Two points need a more detailed explanation